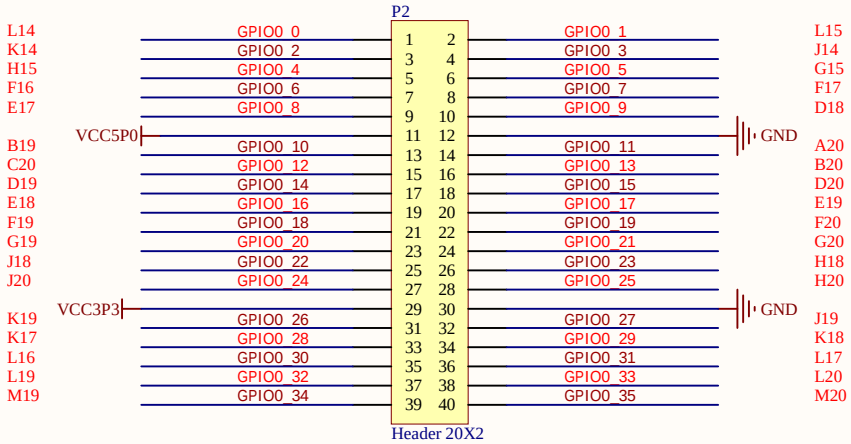
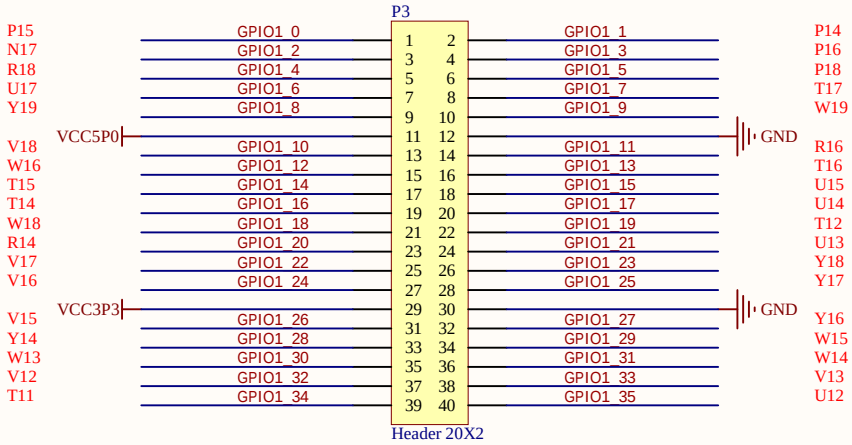
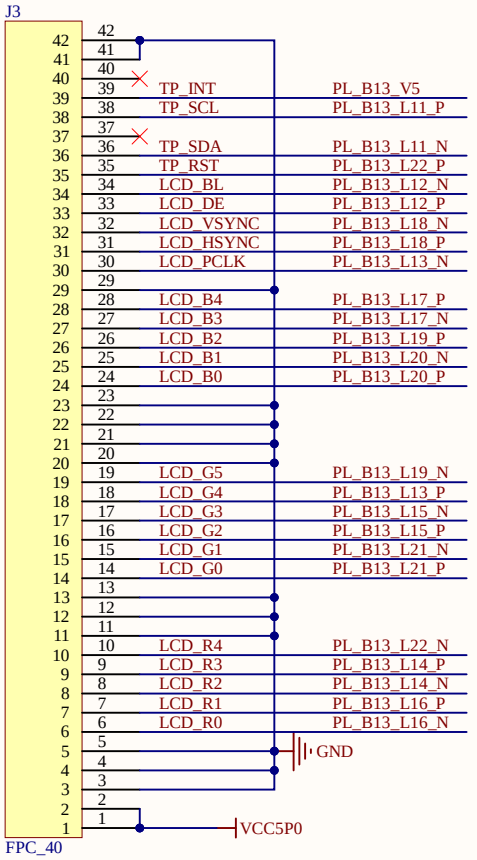


LVDS

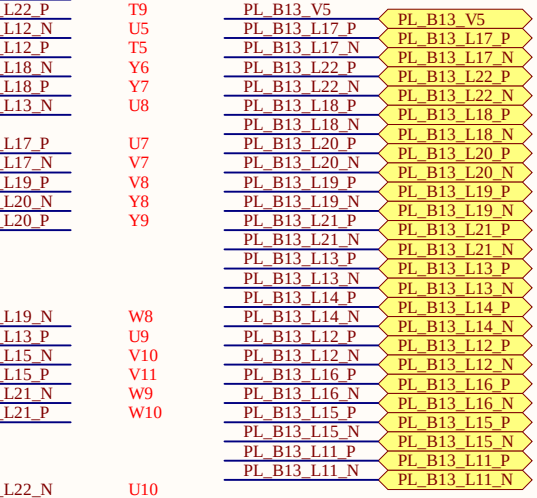


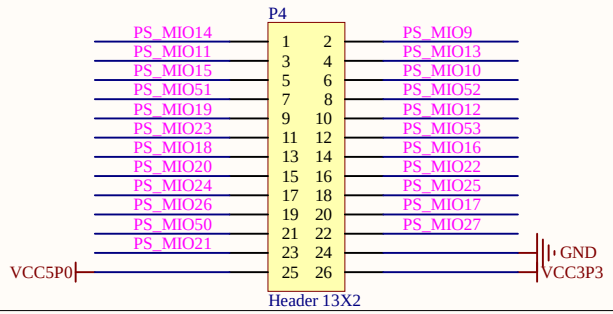
此接口为通用标准扩展接口，兼容友晶DE2开发板扩展口

兼容**DE2**的通用扩展接口



翻盖下接**40P 0.5mm FPC**排线座

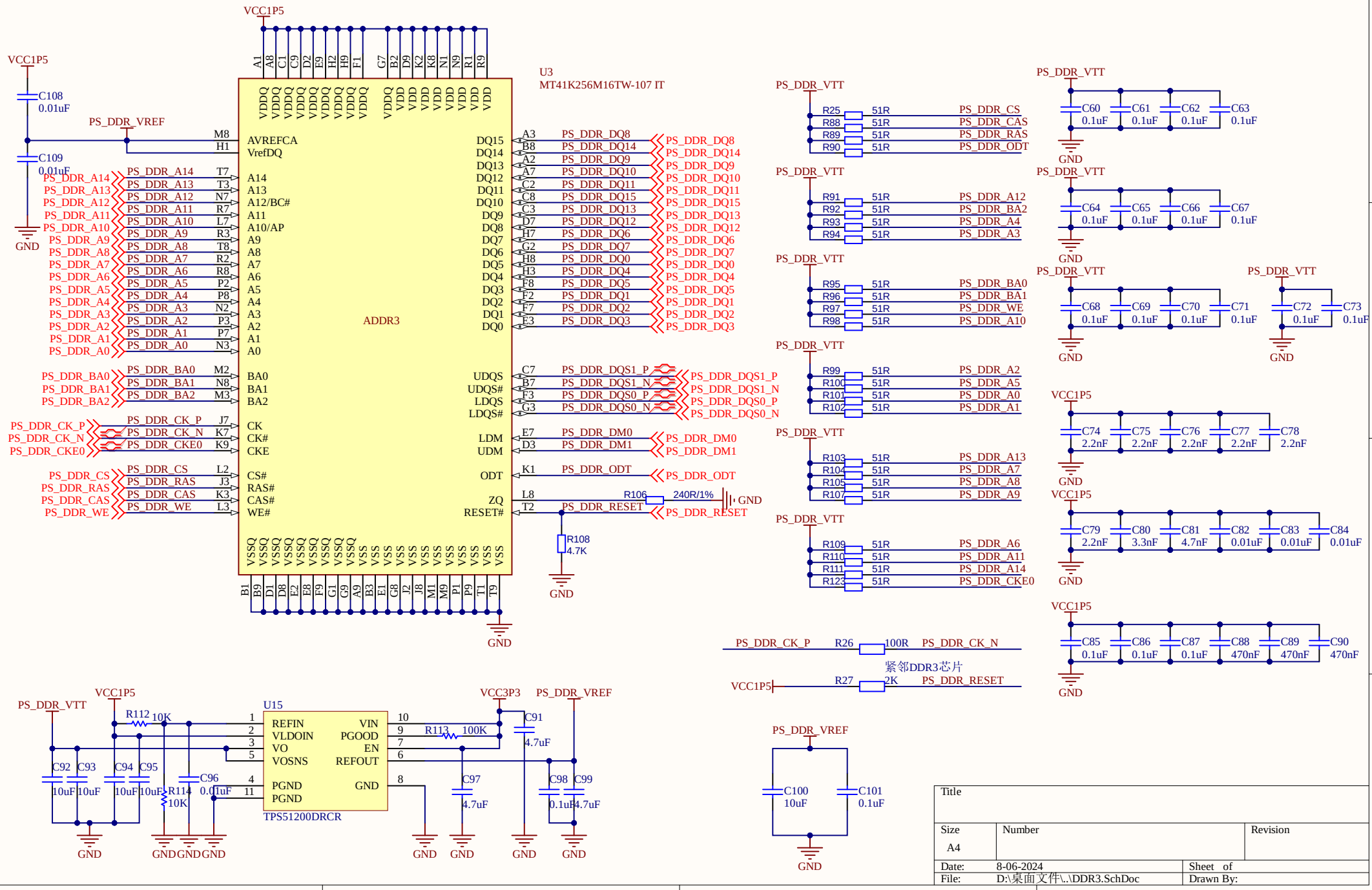


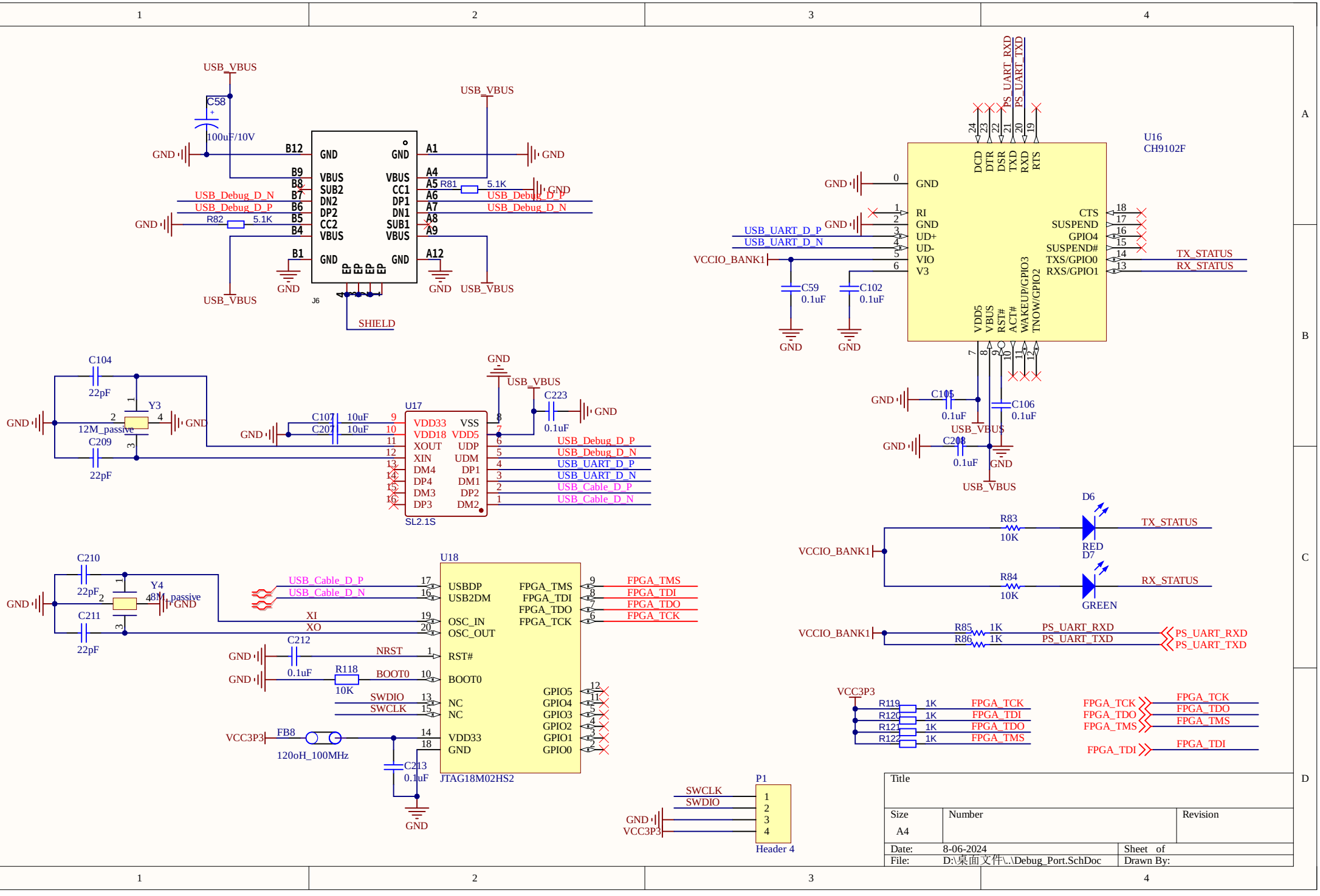


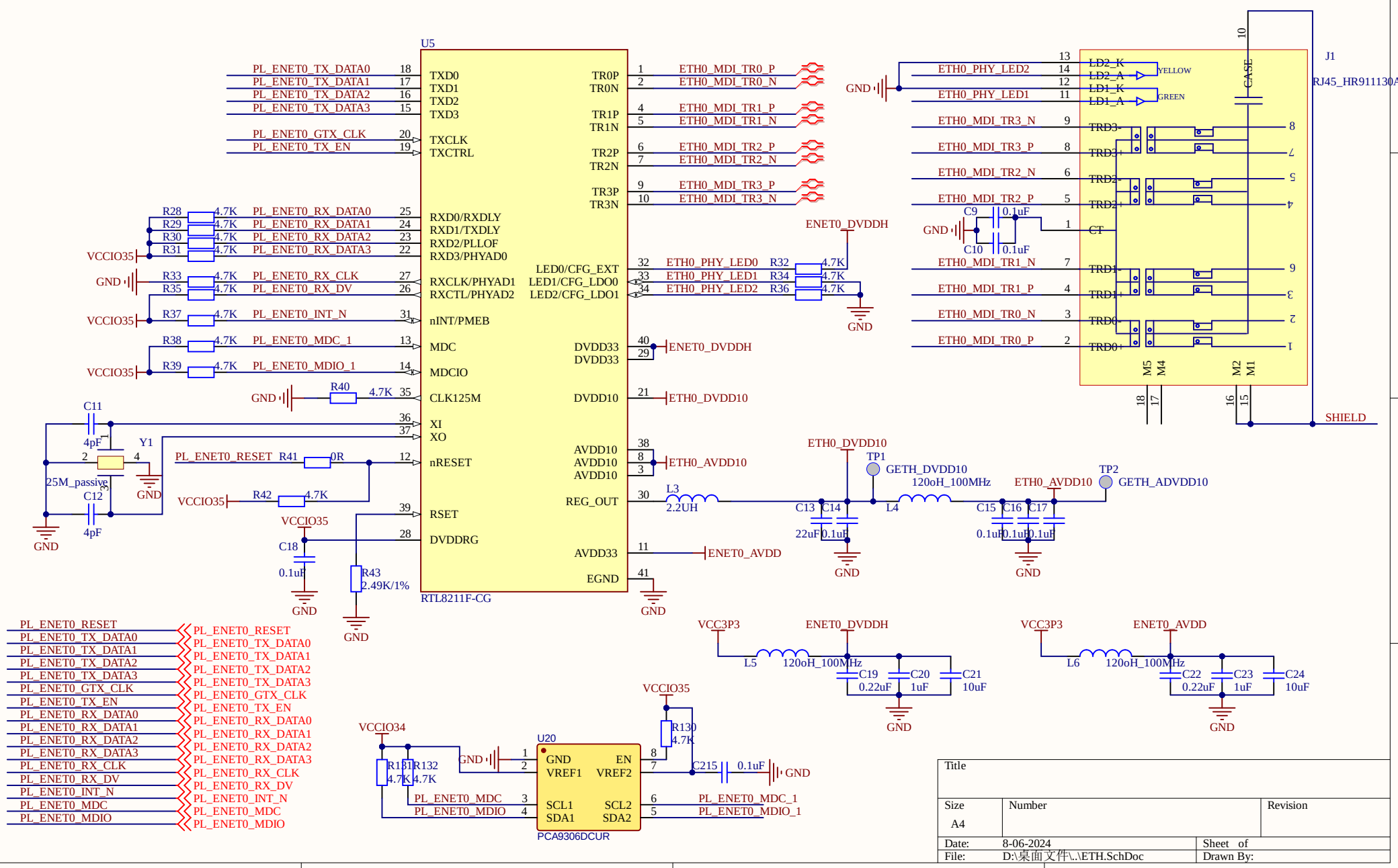
GPIO0_[0..35] GPIO0_[0..35]

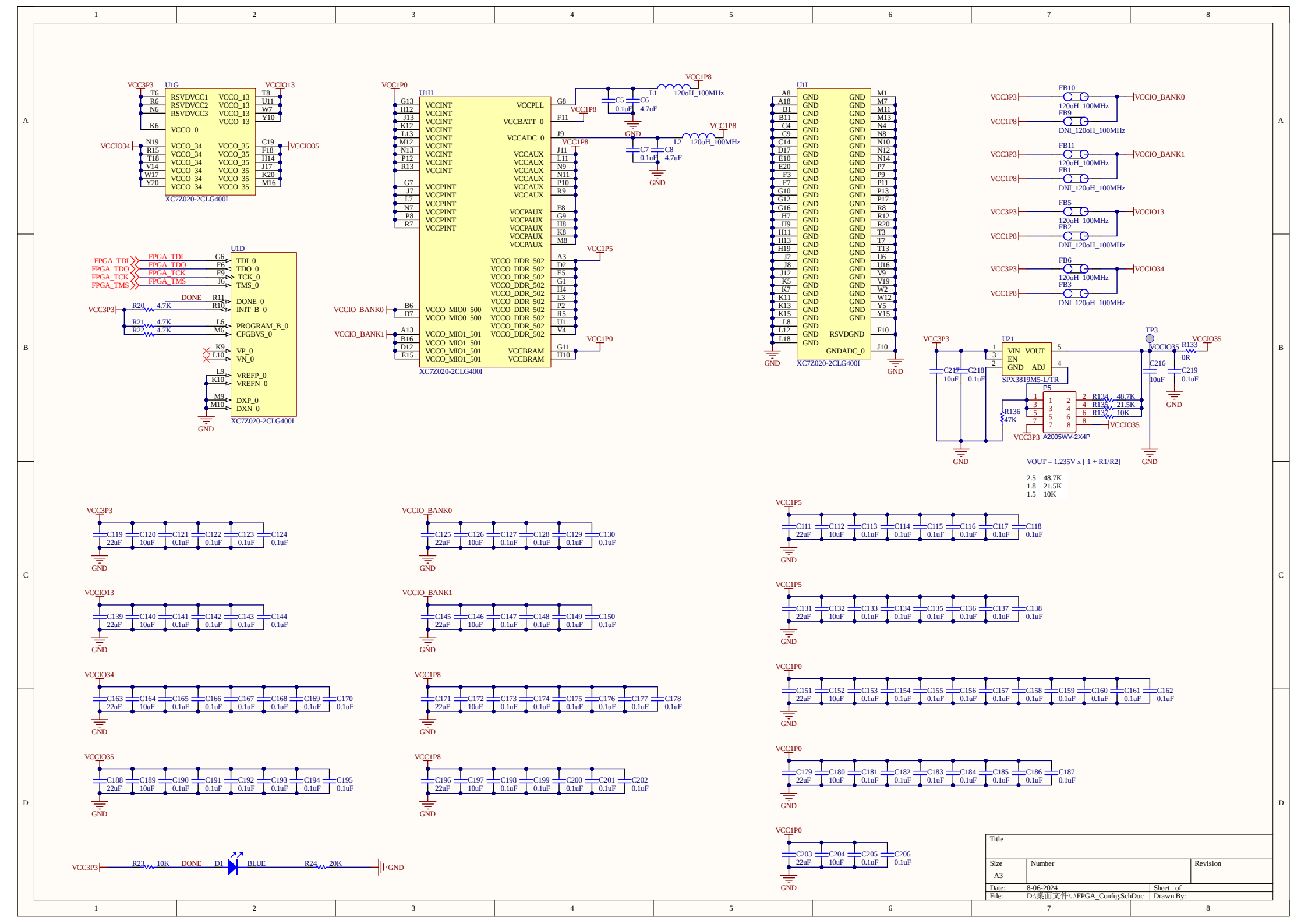
GPIO1_[0..35] GPIO1_[0..35]

Title		
Size A4	Number	Revision
Date: 8-06-2024		Sheet of
File: D:\桌面文件\..\Connector.SchDoc		Drawn By:

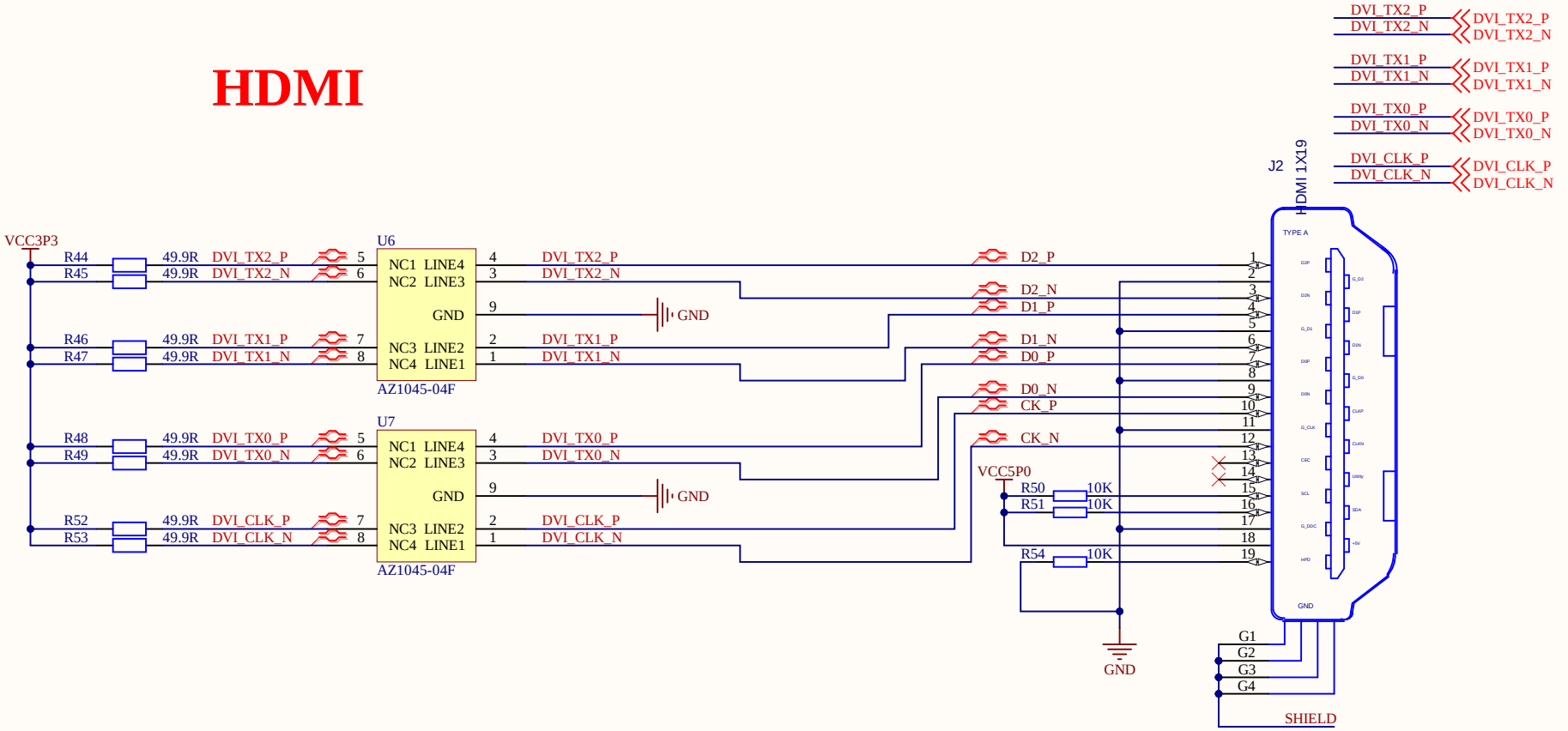

U3
MT41K256M16TW-107 IT
ADDR3
VCC1P5
PS_DDR_VREF
GND
PS_DDR_VTT
PS_DDR_CS
PS_DDR_CAS
PS_DDR_RAS
PS_DDR_ODT
PS_DDR_RESET
R106 240R/1%
R108 4.7K
R26 100R PS_DDR_CK_N
PS_DDR_CK_P
R27 2K
紧邻DDR3芯片
U15
TPS51200DRCR
REFIN
VLDOIN
VO
VOSNS
PGND
VIN
PGOOD
EN
REFOUT
GND
R112 10K
R113 100K
R114 10K
C91 4.7uF
C92 C93 C94 C95 10uF
C96 0.01uF
C97 4.7uF
C98 0.1uF
C99 4.7uF
C100 10uF
C101 0.1uF
Title
Size A4
Number
Revision
Date: 8-06-2024
File: D:\桌面文件\..\DDR3.SchDoc
Sheet of
Drawn By:


USB_VBUS
C58
100uF/10V
GND
B12
B9
B8
B7
B6
B5
B4
B1
A1
A4
A5
A6
A7
A8
A9
A12
R81
5.1K
USB_Debug_D_N
USB_Debug_D_P
R82
SHIELD
J6
C104
22pF
Y3
12M_passive
C209
C107
10uF
C207
U17
VDD33
VDD18
XOUT
XIN
DM4
DP4
DM3
DP3
VSS
VDD5
UDP
UDM
DP1
DM1
DP2
DM2
C223
0.1uF
SL2.1S
C210
Y4
48M_passive
C211
USB_Cable_D_P
USB_Cable_D_N
XI
XO
U18
USBDP
USB2DM
OSC_IN
OSC_OUT
C212
NRST
RST#
R118
10K
BOOT0
SWDIO
SWCLK
NC
FB8
120oH_100MHz
VCC3P3
VDD33
C213
JTAG18M02HS2
FPGA_TMS
FPGA_TDI
FPGA_TDO
FPGA_TCK
GPIO5
GPIO4
GPIO3
GPIO2
GPIO1
GPIO0
P1
Header 4
U16
CH9102F
DCD
DTR
DSR
TXD
RXD
RTS
PS_UART_RXD
PS_UART_TXD
RI
UD+
UD-
VIO
V3
CTS
SUSPEND
GPIO4
SUSPEND#
TXS/GPIO0
RXS/GPIO1
TX_STATUS
RX_STATUS
USB_UART_D_P
USB_UART_D_N
VCCIO_BANK1
C59
C102
VDD5
VBUS
RST#
ACT#
WAKEUP/GPIO3
TNOW/GPIO2
C105
C106
C208
D6
R83
RED
D7
R84
GREEN
R85
R86
1K
R119
R120
R121
R122
Title
Size
A4
Number
Revision
Date:
8-06-2024
Sheet of
File:
D:\桌面文件\..\Debug_Port.SchDoc
Drawn By:

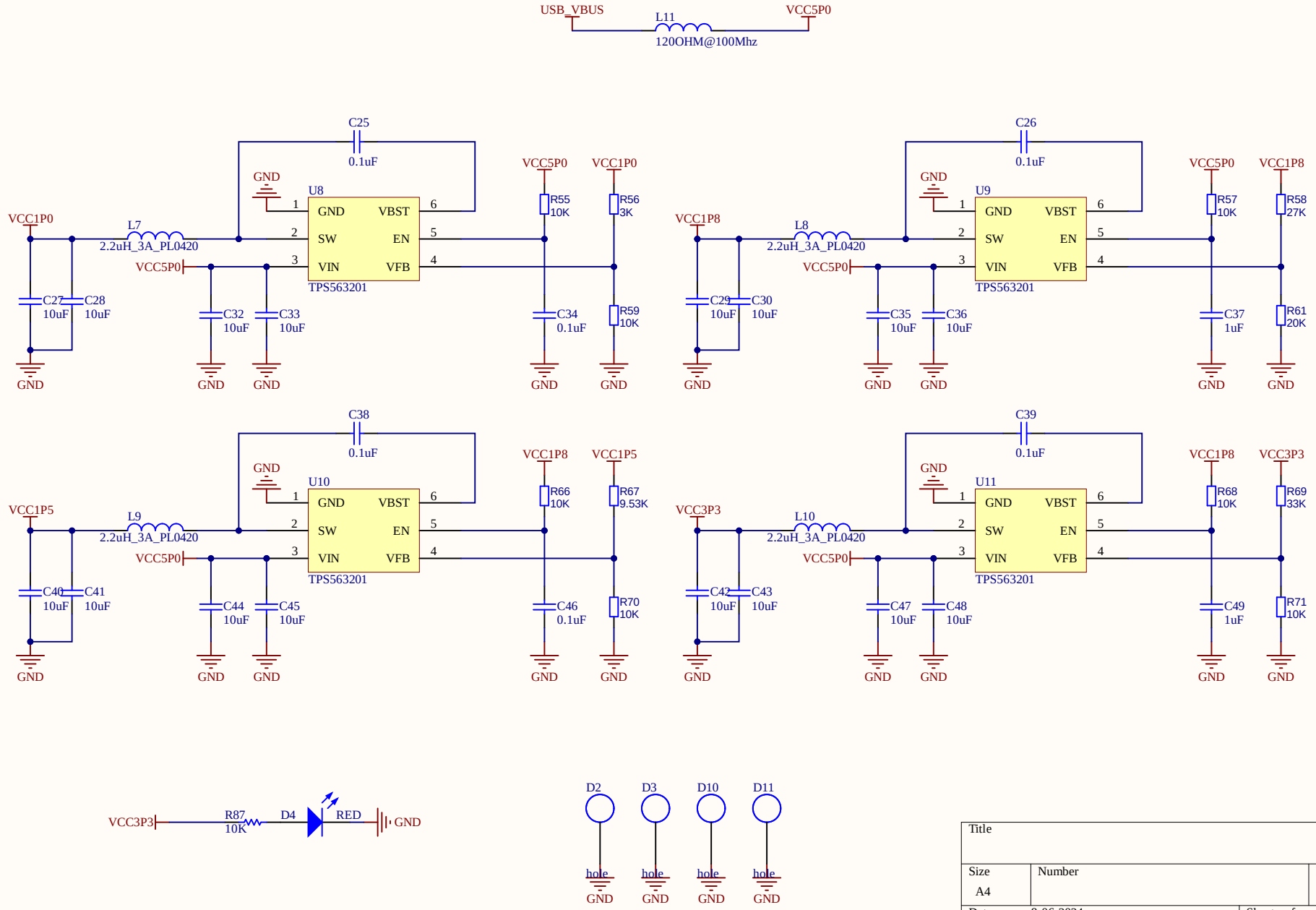

U5
RTL8211F-CG
TXD0
TXD1
TXD2
TXD3
TXCLK
TXCTRL
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOF
RXD3/PHYAD0
RXCLK/PHYAD1
RXCTL/PHYAD2
nINT/PMEB
MDC
MDIO
CLK125M
XI
XO
nRESET
RSET
DVDDRG
TR0P
TR0N
TR1P
TR1N
TR2P
TR2N
TR3P
TR3N
LED0/CFG_EXT
LED1/CFG_LDO0
LED2/CFG_LDO1
DVDD33
DVDD33
DVDD10
AVDD10
AVDD10
AVDD10
REG_OUT
AVDD33
EGND
PL_ENET0_TX_DATA0
PL_ENET0_TX_DATA1
PL_ENET0_TX_DATA2
PL_ENET0_TX_DATA3
PL_ENET0_GTX_CLK
PL_ENET0_TX_EN
PL_ENET0_RX_DATA0
PL_ENET0_RX_DATA1
PL_ENET0_RX_DATA2
PL_ENET0_RX_DATA3
PL_ENET0_RX_CLK
PL_ENET0_RX_DV
PL_ENET0_INT_N
PL_ENET0_MDC_1
PL_ENET0_MDIO_1
PL_ENET0_RESET
ETH0_MDI_TR0_P
ETH0_MDI_TR0_N
ETH0_MDI_TR1_P
ETH0_MDI_TR1_N
ETH0_MDI_TR2_P
ETH0_MDI_TR2_N
ETH0_MDI_TR3_P
ETH0_MDI_TR3_N
ETH0_PHY_LED0
ETH0_PHY_LED1
ETH0_PHY_LED2
ENET0_DVDDH
ETH0_DVDD10
ETH0_AVDD10
ENET0_AVDD
R28 4.7K
R29 4.7K
R30 4.7K
R31 4.7K
R32 4.7K
R33 4.7K
R34 4.7K
R35 4.7K
R36 4.7K
R37 4.7K
R38 4.7K
R39 4.7K
R40 4.7K
R41 0R
R42 4.7K
R43 2.49K/1%
C11 4pF
C12 4pF
Y1 25M_passive
C18 0.1uF
L3 2.2UH
L4 120oH_100MHz
L5 120oH_100MHz
L6 120oH_100MHz
C13 22uF
C14 0.1uF
C15 0.1uF
C16 0.1uF
C17 0.1uF
C19 0.22uF
C20 1uF
C21 10uF
C22 0.22uF
C23 1uF
C24 10uF
TP1 GETH_DVDD10
TP2 GETH_ADVDD10
VCCIO35
VCCIO34
VCC3P3
GND
J1
RJ45_HR911130A
LD2_K
LD2_A
LD1_K
LD1_A
YELLOW
GREEN
CASE
SHIELD
C9 0.1uF
C10 0.1uF
CT
TRD3-
TRD3+
TRD2-
TRD2+
TRD1-
TRD1+
TRD0-
TRD0+
M5
M4
M2
M1
U20
PCA9306DCUR
GND
VREF1
VREF2
EN
SCL1
SDA1
SCL2
SDA2
R130 4.7K
R131 4.7K
R132 4.7K
C215 0.1uF
PL_ENET0_MDC
PL_ENET0_MDIO
PL_ENET0_MDC_1
PL_ENET0_MDIO_1
Title
Size A4
Number
Revision
Date: 8-06-2024
Sheet of
File: D:\桌面文件\..\ETH.SchDoc
Drawn By:


U1G
XC7Z020-2CLG400I
U1H
XC7Z020-2CLG400I
U1I
XC7Z020-2CLG400I
U1D
XC7Z020-2CLG400I
U21
SPX3819M5-L/TR
P5
A2005WV-2X4P
VOUT = 1.235V x [1 + R1/R2]
2.5 48.7K
1.8 21.5K
1.5 10K
Title
Size A3
Number
Revision
Date: 8-06-2024
Sheet of
File: D:\桌面文件\..\FPGA_Config.SchDoc
Drawn By:

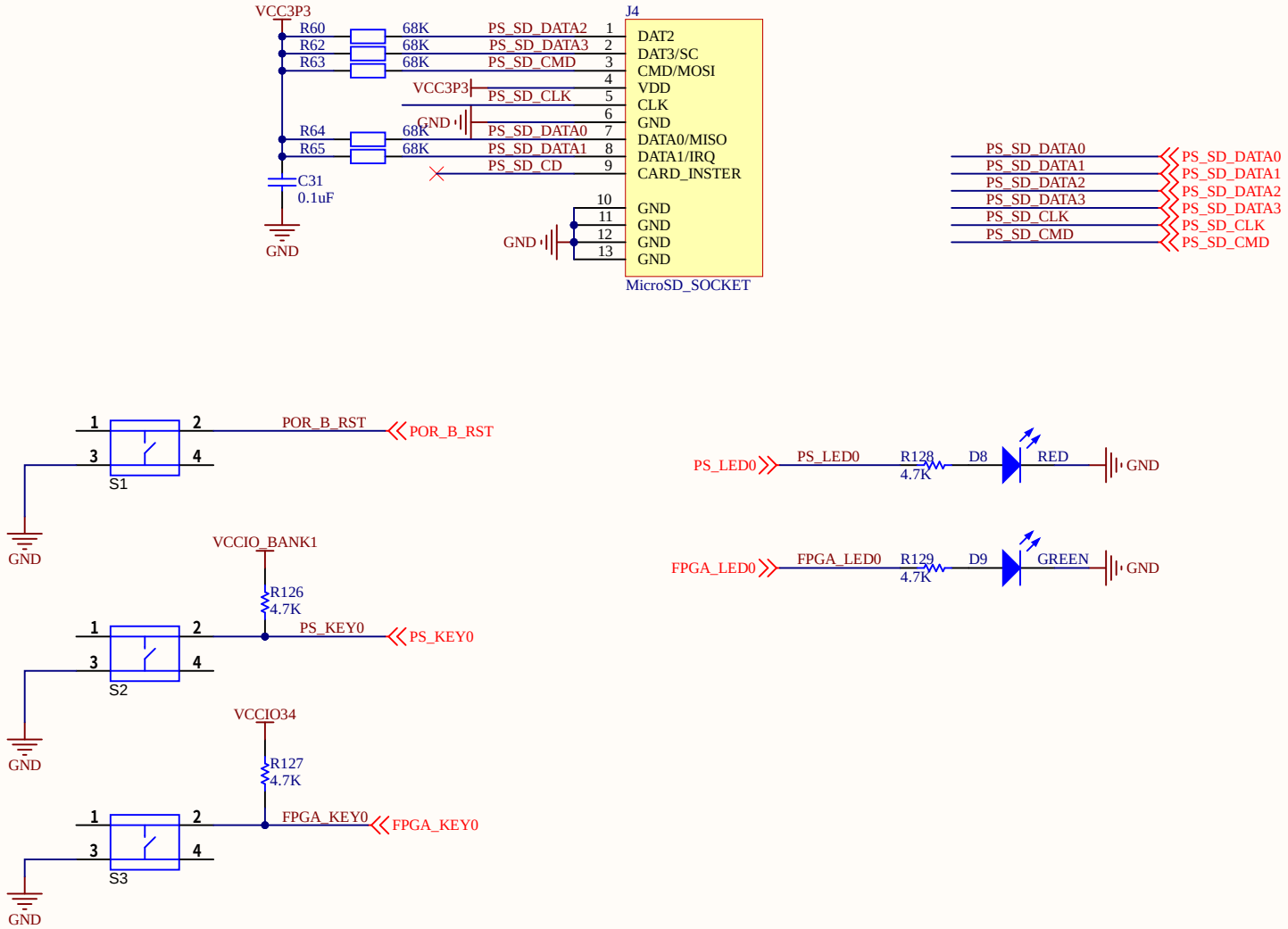
HDMI



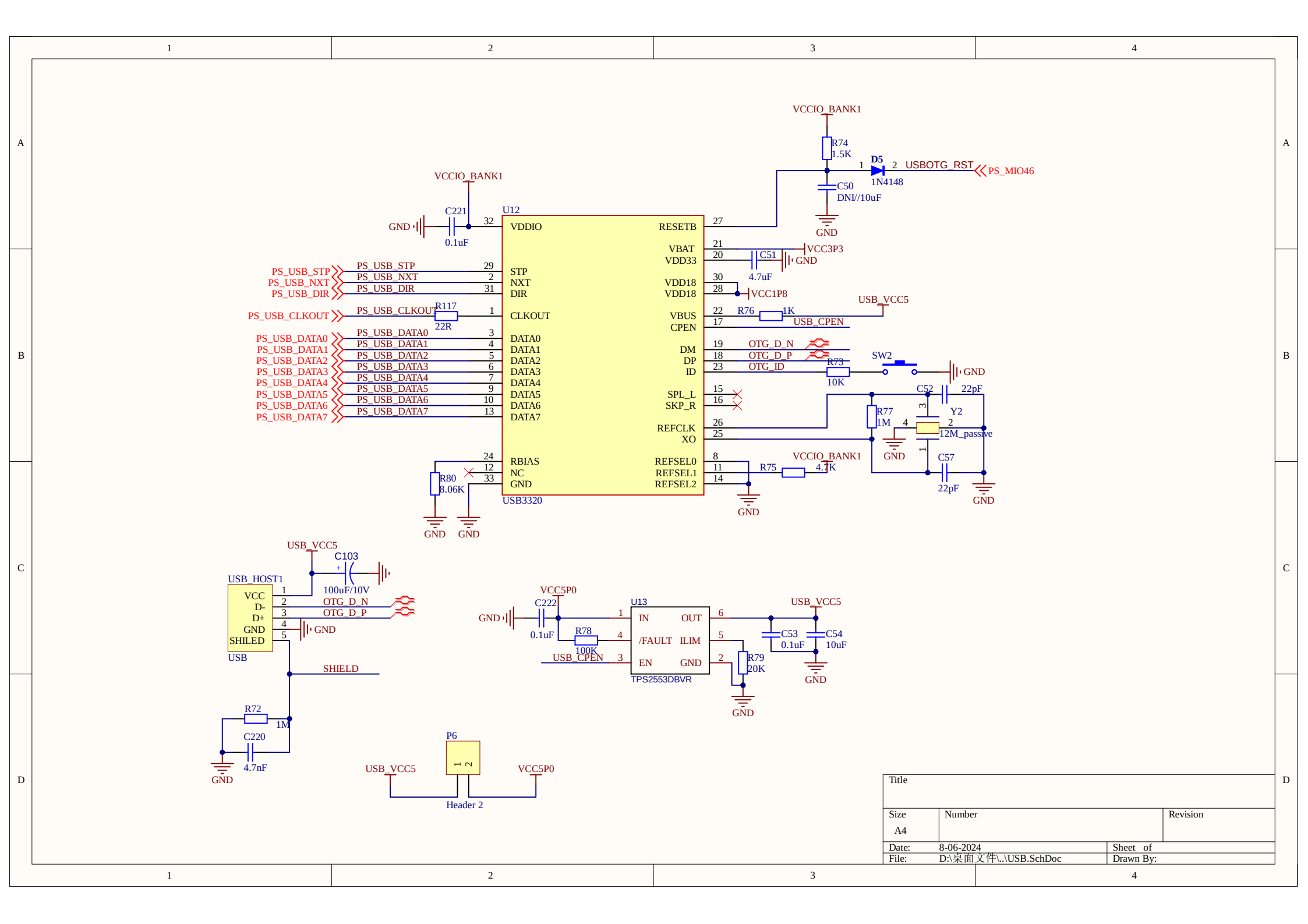
Title		
Size A4	Number	Revision
Date: 8-06-2024		Sheet of
File: D:\桌面文件\..\HDMI.SchDoc		Drawn By:



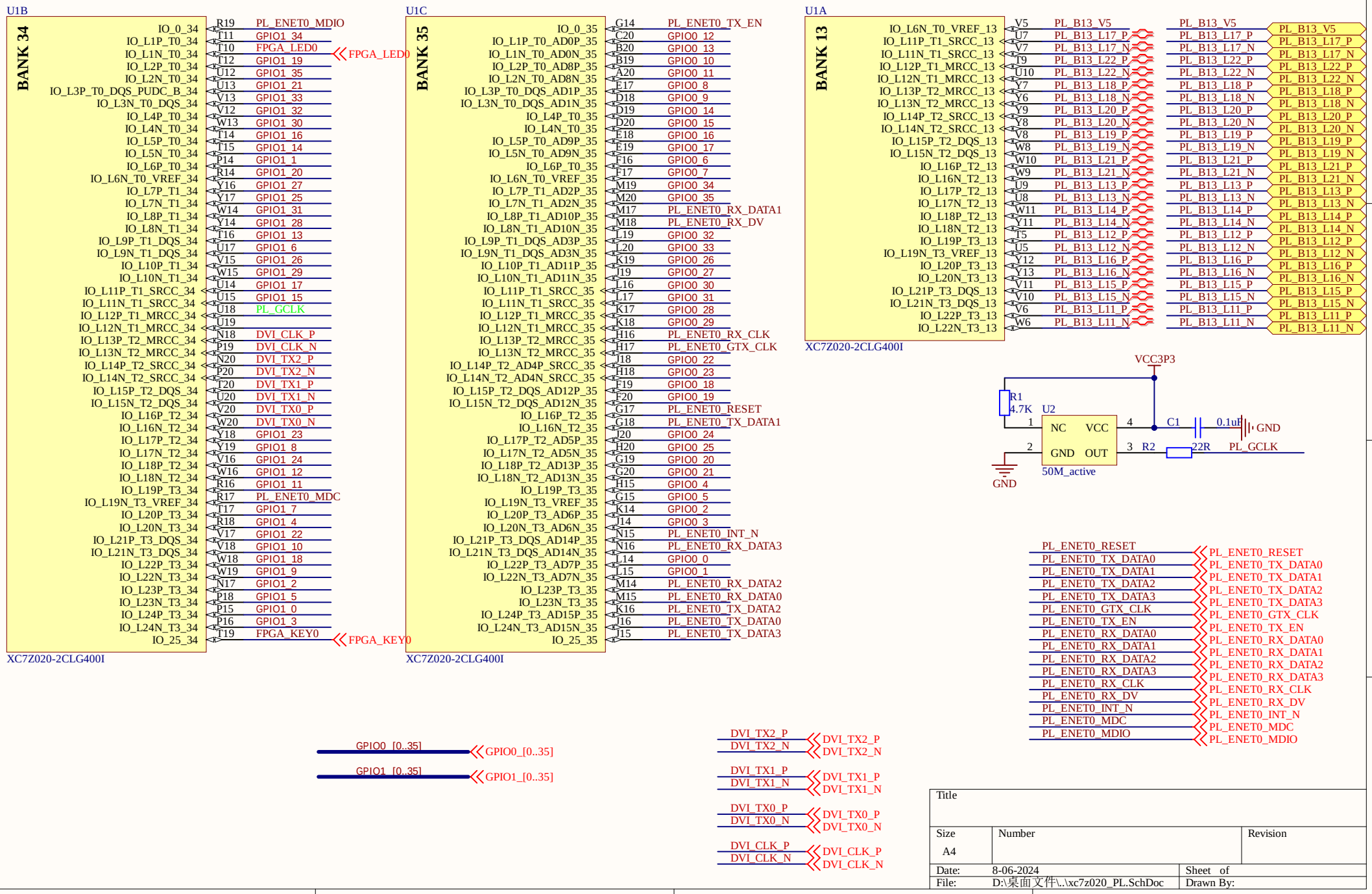
Title		
Size A4	Number	Revision
Date: 8-06-2024		Sheet of
File: D:\桌面文件\..\POWER.SchDoc		Drawn By:

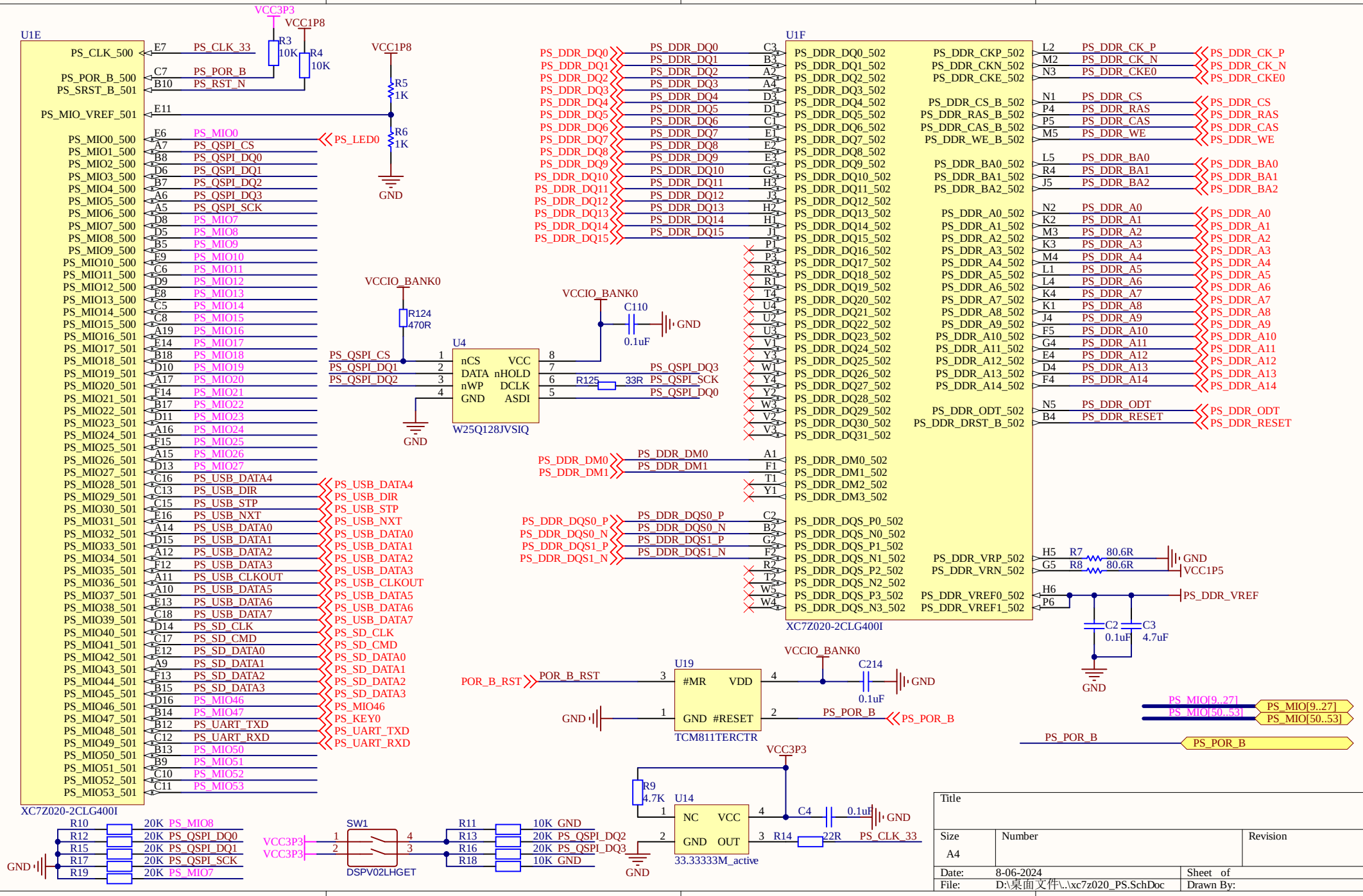


Title		
Size: A4	Number	Revision
Date: 8-06-2024		Sheet of
File: D:\桌面文件\..\SD_CARD.SchDoc		Drawn By:



Title		
Size: A4	Number	Revision
Date: 8-06-2024		Sheet of
File: D:\桌面文件\..\USB.SchDoc		Drawn By:


U1B
BANK 34
IO_0_34 R19 PL_ENET0_MDIO
IO_L1P_T0_34 T11 GPIO1_34
IO_L1N_T0_34 T10 FPGA_LED0
IO_L2P_T0_34 T12 GPIO1_19
IO_L2N_T0_34 U12 GPIO1_35
IO_L3P_T0_DQS_PUDC_B_34 U13 GPIO1_21
IO_L3N_T0_DQS_34 V13 GPIO1_33
IO_L4P_T0_34 V12 GPIO1_32
IO_L4N_T0_34 W13 GPIO1_30
IO_L5P_T0_34 T14 GPIO1_16
IO_L5N_T0_34 T15 GPIO1_14
IO_L6P_T0_34 P14 GPIO1_1
IO_L6N_T0_VREF_34 R14 GPIO1_20
IO_L7P_T1_34 Y16 GPIO1_27
IO_L7N_T1_34 Y17 GPIO1_25
IO_L8P_T1_34 W14 GPIO1_31
IO_L8N_T1_34 Y14 GPIO1_28
IO_L9P_T1_DQS_34 T16 GPIO1_13
IO_L9N_T1_DQS_34 U17 GPIO1_6
IO_L10P_T1_34 V15 GPIO1_26
IO_L10N_T1_34 W15 GPIO1_29
IO_L11P_T1_SRCC_34 U14 GPIO1_17
IO_L11N_T1_SRCC_34 U15 GPIO1_15
IO_L12P_T1_MRCC_34 U18 PL_GCLK
IO_L12N_T1_MRCC_34 U19
IO_L13P_T2_MRCC_34 N18 DVI_CLK_P
IO_L13N_T2_MRCC_34 P19 DVI_CLK_N
IO_L14P_T2_SRCC_34 N20 DVI_TX2_P
IO_L14N_T2_SRCC_34 P20 DVI_TX2_N
IO_L15P_T2_DQS_34 T20 DVI_TX1_P
IO_L15N_T2_DQS_34 U20 DVI_TX1_N
IO_L16P_T2_34 V20 DVI_TX0_P
IO_L16N_T2_34 W20 DVI_TX0_N
IO_L17P_T2_34 Y18 GPIO1_23
IO_L17N_T2_34 Y19 GPIO1_8
IO_L18P_T2_34 V16 GPIO1_24
IO_L18N_T2_34 W16 GPIO1_12
IO_L19P_T3_34 R16 GPIO1_11
IO_L19N_T3_VREF_34 R17 PL_ENET0_MDC
IO_L20P_T3_34 T17 GPIO1_7
IO_L20N_T3_34 R18 GPIO1_4
IO_L21P_T3_DQS_34 V17 GPIO1_22
IO_L21N_T3_DQS_34 V18 GPIO1_10
IO_L22P_T3_34 W18 GPIO1_18
IO_L22N_T3_34 W19 GPIO1_9
IO_L23P_T3_34 N17 GPIO1_2
IO_L23N_T3_34 P18 GPIO1_5
IO_L24P_T3_34 P15 GPIO1_0
IO_L24N_T3_34 P16 GPIO1_3
IO_25_34 T19 FPGA_KEY0
FPGA_LED0
FPGA_KEY0
XC7Z020-2CLG400I
U1C
BANK 35
IO_0_35 G14 PL_ENET0_TX_EN
IO_L1P_T0_AD0P_35 C20 GPIO0_12
IO_L1N_T0_AD0N_35 B20 GPIO0_13
IO_L2P_T0_AD8P_35 B19 GPIO0_10
IO_L2N_T0_AD8N_35 A20 GPIO0_11
IO_L3P_T0_DQS_AD1P_35 E17 GPIO0_8
IO_L3N_T0_DQS_AD1N_35 D18 GPIO0_9
IO_L4P_T0_35 D19 GPIO0_14
IO_L4N_T0_35 D20 GPIO0_15
IO_L5P_T0_AD9P_35 E18 GPIO0_16
IO_L5N_T0_AD9N_35 E19 GPIO0_17
IO_L6P_T0_35 F16 GPIO0_6
IO_L6N_T0_VREF_35 F17 GPIO0_7
IO_L7P_T1_AD2P_35 M19 GPIO0_34
IO_L7N_T1_AD2N_35 M20 GPIO0_35
IO_L8P_T1_AD10P_35 M17 PL_ENET0_RX_DATA1
IO_L8N_T1_AD10N_35 M18 PL_ENET0_RX_DV
IO_L9P_T1_DQS_AD3P_35 L19 GPIO0_32
IO_L9N_T1_DQS_AD3N_35 L20 GPIO0_33
IO_L10P_T1_AD11P_35 K19 GPIO0_26
IO_L10N_T1_AD11N_35 J19 GPIO0_27
IO_L11P_T1_SRCC_35 L16 GPIO0_30
IO_L11N_T1_SRCC_35 L17 GPIO0_31
IO_L12P_T1_MRCC_35 K17 GPIO0_28
IO_L12N_T1_MRCC_35 K18 GPIO0_29
IO_L13P_T2_MRCC_35 H16 PL_ENET0_RX_CLK
IO_L13N_T2_MRCC_35 H17 PL_ENET0_GTX_CLK
IO_L14P_T2_AD4P_SRCC_35 J18 GPIO0_22
IO_L14N_T2_AD4N_SRCC_35 H18 GPIO0_23
IO_L15P_T2_DQS_AD12P_35 F19 GPIO0_18
IO_L15N_T2_DQS_AD12N_35 F20 GPIO0_19
IO_L16P_T2_35 G17 PL_ENET0_RESET
IO_L16N_T2_35 G18 PL_ENET0_TX_DATA1
IO_L17P_T2_AD5P_35 J20 GPIO0_24
IO_L17N_T2_AD5N_35 H20 GPIO0_25
IO_L18P_T2_AD13P_35 G19 GPIO0_20
IO_L18N_T2_AD13N_35 G20 GPIO0_21
IO_L19P_T3_35 H15 GPIO0_4
IO_L19N_T3_VREF_35 G15 GPIO0_5
IO_L20P_T3_AD6P_35 K14 GPIO0_2
IO_L20N_T3_AD6N_35 J14 GPIO0_3
IO_L21P_T3_DQS_AD14P_35 N15 PL_ENET0_INT_N
IO_L21N_T3_DQS_AD14N_35 N16 PL_ENET0_RX_DATA3
IO_L22P_T3_AD7P_35 L14 GPIO0_0
IO_L22N_T3_AD7N_35 L15 GPIO0_1
IO_L23P_T3_35 M14 PL_ENET0_RX_DATA2
IO_L23N_T3_35 M15 PL_ENET0_RX_DATA0
IO_L24P_T3_AD15P_35 K16 PL_ENET0_TX_DATA2
IO_L24N_T3_AD15N_35 J16 PL_ENET0_TX_DATA0
IO_25_35 J15 PL_ENET0_TX_DATA3
XC7Z020-2CLG400I
U1A
BANK 13
IO_L6N_T0_VREF_13 V5 PL_B13_V5
IO_L1P_T1_SRCC_13 U7 PL_B13_L17_P
IO_L1N_T1_SRCC_13 V7 PL_B13_L17_N
IO_L12P_T1_MRCC_13 T9 PL_B13_L22_P
IO_L12N_T1_MRCC_13 U10 PL_B13_L22_N
IO_L13P_T2_MRCC_13 Y7 PL_B13_L18_P
IO_L13N_T2_MRCC_13 Y6 PL_B13_L18_N
IO_L14P_T2_SRCC_13 Y9 PL_B13_L20_P
IO_L14N_T2_SRCC_13 Y8 PL_B13_L20_N
IO_L15P_T2_DQS_13 V8 PL_B13_L19_P
IO_L15N_T2_DQS_13 W8 PL_B13_L19_N
IO_L16P_T2_13 W10 PL_B13_L21_P
IO_L16N_T2_13 W9 PL_B13_L21_N
IO_L17P_T2_13 U9 PL_B13_L13_P
IO_L17N_T2_13 U8 PL_B13_L13_N
IO_L18P_T2_13 W11 PL_B13_L14_P
IO_L18N_T2_13 Y11 PL_B13_L14_N
IO_L19P_T3_13 T5 PL_B13_L12_P
IO_L19N_T3_VREF_13 U5 PL_B13_L12_N
IO_L20P_T3_13 Y12 PL_B13_L16_P
IO_L20N_T3_13 Y13 PL_B13_L16_N
IO_L21P_T3_DQS_13 V11 PL_B13_L15_P
IO_L21N_T3_DQS_13 V10 PL_B13_L15_N
IO_L22P_T3_13 V6 PL_B13_L11_P
IO_L22N_T3_13 W6 PL_B13_L11_N
PL_B13_V5
PL_B13_L17_P
PL_B13_L17_N
PL_B13_L22_P
PL_B13_L22_N
PL_B13_L18_P
PL_B13_L18_N
PL_B13_L20_P
PL_B13_L20_N
PL_B13_L19_P
PL_B13_L19_N
PL_B13_L21_P
PL_B13_L21_N
PL_B13_L13_P
PL_B13_L13_N
PL_B13_L14_P
PL_B13_L14_N
PL_B13_L12_P
PL_B13_L12_N
PL_B13_L16_P
PL_B13_L16_N
PL_B13_L15_P
PL_B13_L15_N
PL_B13_L11_P
PL_B13_L11_N
XC7Z020-2CLG400I
VCC3P3
R1
4.7K
U2
NC
VCC
GND
OUT
50M_active
C1
0.1uF
GND
R2
22R
PL_GCLK
GND
PL_ENET0_RESET
PL_ENET0_TX_DATA0
PL_ENET0_TX_DATA1
PL_ENET0_TX_DATA2
PL_ENET0_TX_DATA3
PL_ENET0_GTX_CLK
PL_ENET0_TX_EN
PL_ENET0_RX_DATA0
PL_ENET0_RX_DATA1
PL_ENET0_RX_DATA2
PL_ENET0_RX_DATA3
PL_ENET0_RX_CLK
PL_ENET0_RX_DV
PL_ENET0_INT_N
PL_ENET0_MDC
PL_ENET0_MDIO
GPIO0_[0..35]
GPIO1_[0..35]
DVI_TX2_P
DVI_TX2_N
DVI_TX1_P
DVI_TX1_N
DVI_TX0_P
DVI_TX0_N
DVI_CLK_P
DVI_CLK_N
Title
Size
A4
Number
Revision
Date: 8-06-2024
Sheet of
File: D:\桌面文件\..\xc7z020_PL.SchDoc
Drawn By:


U1E
XC7Z020-2CLG400I
U1F
XC7Z020-2CLG400I
U4
W25Q128JVSIQ
U19
TCM811TERCTR
U14
33.33333M_active
SW1
DSPV02LHGET
VCC3P3
VCC1P8
VCCIO_BANK0
GND
PS_LED0
PS_QSPI_CS
PS_QSPI_DQ0
PS_QSPI_DQ1
PS_QSPI_DQ2
PS_QSPI_DQ3
PS_QSPI_SCK
PS_POR_B
POR_B_RST
PS_CLK_33
PS_DDR_VRP_502
PS_DDR_VRN_502
PS_DDR_VREF
VCC1P5
Title
Size
A4
Number
Revision
Date: 8-06-2024
File: D:\桌面文件\..\xc7z020_PS.SchDoc
Sheet of
Drawn By: